HEWLETT PACKARD

APPLICATION NOTE 989

Step Recovery Diode Doubler

INTRODUCTION

A straightforward technique for multiplier design is presented. The input circuit is a low pass filter which allows all of the input power to be absorbed by the diode and reflects harmonic power back to the diode. The output circuit is a bandpass filter which offers a low loss path to the desired frequency while reflecting all other harmonics back to the diode.

FREQUENCY MULTIPLICATION WITH STEP RECOVERY DIODES

A step recovery diode has two operating states. With forward bias it looks like a large capacitor — a low impedance. Under reverse bias it looks like a small capacitor — a high impedance. However, the diode is a three layer device and charge can be injected and stored in one of these layers, the I (intrinsic) layer, when forward bias is applied. The change from low impedance to high impedance does not take place until reverse current flows long enough to remove the charge. The change then takes place quickly, in a time interval called the diode transition time.

This sudden change in diode resistance causes a sudden change in current through the final inductor of the low pass filter. This produces a narrow pulse of voltage which is equivalent to a number of frequencies which are multiples of the input frequency. The highest multiple is limited by the narrowness of the pulse which is determined by the transition time. The multiplier is completed by adding a bandpass filter to pass the desired multiple and reflect all others. By properly spacing the multiplier from the filter, much of the power in these unwanted frequencies can be converted to the desired output[1].

BIAS CURRENT

For maximum efficiency the sudden change of diode resistance should occur at the negative peak of the input waveform. This is controlled by providing negative DC bias to the diode to set the time when conduction starts during the position portion of the input wave. This bias voltage may be provided by a resistor across the input circuit. Rectified current from the diode flows through the bias resistor to generate the negative bias voltage. The proper value of bias resistance is[2]

$$R_B = \frac{2\tau}{\pi N^2 C}$$

where τ is the lifetime, 100×10^{-9} seconds, N is the multiplication factor, and C is the diode capacitance, 3 pF, so that R_B = 5300 ohms.

The major effect of temperature on step recovery diodes is an increase of lifetime of 0.5%/° C. This is easily compensated by using a silicon resistor, a sensistor, for the bias resistor. Sensistors with this temperature sensitivity are available.

DIODE CHOICE

The design technique will be illustrated by a doubler from 2 to 4 GHz. In the Hewlett-Packard Diode Designer's Catalog the 5082-0805 Step Recovery Diode is recommended for a 4 GHz output frequency. This fits the multiplier rule that the transition time should be equal to or less than the inverse of the output frequency. In this case the typical transition time is 250 picoseconds, the inverse of the 4 GHz output frequency.

A similar rule relates input frequency to lifetime. The lifetime should exceed the inverse of the input frequency. Since the lifetime always exceeds the transition time by a factor of several hundred, this lifetime limitation is not important for low order multipliers.

In some multiplier applications, the breakdown voltage limits the output power. However, for a CW doubler to 4 GHz, the thermal resistance, θ_{jc}, is the limiting factor.

$$P_{MAX} = \frac{200 - T}{\theta_{jc}}$$

For an ambient temperature, T, of 25° C, and θ_{jc} = 20° C/W, P_{MAX} = 8.8 watts. In pulse applications, where the thermal resistance is not the limiting factor, the breakdown voltage limits the power output[3].

$$P_{MAX} = 0.4\, f_{OUT}\, C_j\, V_B^2$$

For a 3 pF junction capacitance, 4 GHz output frequency, and 75 volts breakdown, power output is limited to 27 watts.

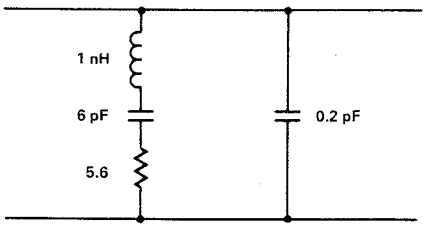

Figure 1. Diode Equivalent Circuit

DIODE EQUIVALENT CIRCUIT

The diode chip is represented by a capacitor in series with a resistor[4]. The capacitance is double the value measured at 1 MHz with reverse voltage. In this case, 2x3 pF = 6 pF. The resistance is computed from the input frequency ω_{in} and the reverse bias junction capacitance C_{min} with the formula

$$\frac{0.21}{\omega_{in}\, C_{min}} = 5.6 \text{ ohms}$$

The rest of the diode circuit includes 1 nH package inductance and 0.2 pF package capacitance as shown in Figure 1.

INPUT FILTER

The initial design of the input filter is based on a low pass impedance transforming network using a lumped element prototype[5] shown in Figure 2. The diode impedance at 2 GHz is 5.61 - j 0.77. The prototype is normalized to unity generator impedance so the load conductance g5 is

$$r = \frac{50}{5.6} = 8.9$$

The series element g_4 will be modified later to include the load reactance.

The number of filter elements is determined by the impedance transformation ratio r (8.9), the bandwidth, and the desired passband ripple.

A bandwidth from 1.9 GHz to 2.1 GHz was chosen with a ripple less than 0.04 dB (SWR = 1.2). Table 2 in the Matthaei article shows that a four element filter as shown in Figure 2 will easily satisfy these requirements. Table 7 provides g_1 = 1.54 and g_2 = 0.61. The other elements are $g_3 = g_2$, r = 5.4 and

$$g_4 = \frac{g_1}{r} = 0.17$$

This prototype assumes a center angular frequency of unity as well as a one ohm generator. Normalization is removed by changing generator and load to 50 ohms and 5.6 ohms, dividing g_1 and g_3 by 50, multiplying g_2 and g_4 by 50 and dividing all elements by the center frequncy $\omega = 2\pi \times 2 \times 10^9$. The lumped element filter now consists of:

$$C_1 = \frac{g_1}{50\omega} = 2.45 \text{ pF} \qquad C_3 = \frac{g_3}{50\omega} = 8.6 \text{ pF}$$

$$L_2 = \frac{50\, g_2}{\omega} = 2.43 \text{ nH} \qquad L_4 = \frac{50\, g_4}{\omega} = 0.68 \text{ nH}$$

Since the diode impedance at 2 GHz is 5.61 - j 0.77, the value of L_4 must be increased by 0.06 nH to cancel the diode reactance.

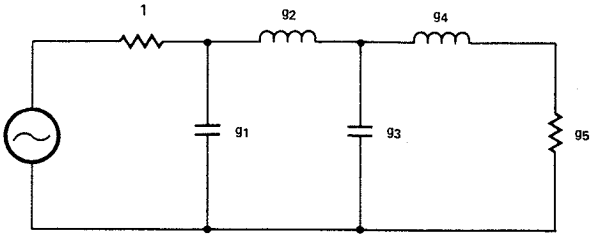

Figure 2. Low Pass Prototype for Input Filter

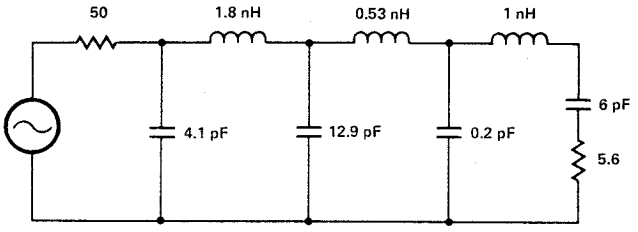

Figure 3. Optimized Lumped Element Low Pass Filter

When this modified filter is used with the diode equivalent circuit of Figure 1 the maximum SWR is 1.3 because the modification of L_4 is valid only at the center frequency. Figure 3 shows the filter optimized by the Compact[6] computer program to reduce the maximum SWR to 1.09.

LUMPED ELEMENTS TO SERIES TRANSMISSION LINES

It is often possible to transform lumped elements to equivalent series transmission lines which are easier to realize in microstrip circuits. However, the validity of this substitution depends on the size of the load impedance and the size of the lumped element.

Consider the possibility of substituting a length, θ, of transmission line of characteristic impedance Z_o for a series inductance L which is followed by a load impedance Z_L. This is valid when

$$Z_o \frac{Z_L + jZ_o \tan\theta}{Z_o + jZ_L \tan\theta} = Z_L + j\omega L$$

If $Z_L \tan\theta << Z_o$ and θ is small so that $\tan\theta = \theta = \frac{\omega \ell}{\nu}$, then this expression simplifies to

$$Z_o \frac{\omega \ell}{\nu} = \omega L$$

$$\ell = \frac{L\nu}{Z_o}$$

where ω = angular frequency
ℓ = length of transmission line
and ν = velocity of propagation

The requirement that $\tan\theta = \theta$ assures that the substitution is valid over a range of frequencies. This means that the transmission line must be short, θ less than 0.5 radian. The other equation limits the size of the load impedance.

$$Z_L\theta << Z_o$$

If we accept 80 ohms as the largest reasonable characteristic impedance, then $Z_L\theta$ should be no more than 8 ohms so that $Z_L\theta << 80$. In the worst case $\theta = 0.5$, Z_L should be less than 16 ohms.

Consider $L_4 = 0.53$ nH terminated with the diode impedance 5.6 - j 0.8. Since the load impedance is small we can replace L_4 with an 80 ohm microstrip line with length in alumina

$$(v = \frac{c}{\sqrt{\epsilon}} = \frac{30}{2.45} \text{ cm/ns})$$

$$\ell = \frac{Lv}{Z_o} = \frac{0.53 \times 30}{80 \times 2.45} = 0.081 \text{ cm } (.032 \text{ inch})$$

or 4.8 degrees.

Similarly the load seen by L_2 is small so L_2 can be replaced by an 80 ohm line of length

$$\frac{1.8 \times 30}{80 \times 2.45} = 0.28 \text{ cm } (0.11 \text{ inch})$$

or 16.1 degrees.

Similar analysis of the shunt elements leads to the requirement

$$Y_L << Y_o/\theta$$

The admittance of the diode plus L_4 is 0.085 - j 0.089 at 2 GHz. The largest reasonable value of Y_o, corresponding to 20 ohms characteristic impedance, is 0.05 so this condition is not satisfied unless the line length is extremely short, about 3°.

The equivalent line requires $1000\, Y_o\, \ell = Cv$. For C = 12.9 pF

$$\ell = \frac{12.9 \times 30 \times 20}{1000 \times 2.75} = 2.81 \text{ cm}$$

or 3.2 radians. This is much longer than 0.5 radian so a series length of line is not a good approximation for this shunt capacitor.

OPEN LINES FOR CAPACITORS

Each shunt capacitor may be represented by a pair of shunt open lines with the relationship

$$Y_o \tan\theta = \frac{\omega C}{2}$$

Use a large Y_o, 0.05, to keep θ as small as possible. For C = 12.9 pF

$$\tan\theta = \frac{20 \times 4\pi \times 12.2}{2000} = 1.62$$

$$\theta = 58.3°$$

For C = 4.1 pF, $\theta = 27.3°$.

Replacing lumped elements with distributed elements has little effect on maximum SWR. Optimization of the open lengths results in less than 10% change and a maximum SWR of 1.09.

EFFECT OF INPUT FILTER ON DESIGN OF OUTPUT FILTER

Before proceeding with the output filter design, we should compute the effect of this low pass filter on the diode impedance at the output frequency.

At 4 GHz the input filter from the diode looks like 0.66 nH. This changes the diode impedance from 6.8 + j20 to 1.4 + j9.8. An unsuccessful attempt was made to modify the filter elements to provide an open circuit at 4 GHz while maintaining a match to the diode at the input frequency band. However, this was successfully accomplished by adding shunt open lines at the diode to resonate the filter at 4 GHz. These lines are 30° long at 4 GHz with 20 ohm characteristic impedance. The effect at the input frequency is small. Maximum SWR for 1900 MHz to 2100 MHz goes up from 1.09 to 1.10.

OUTPUT FILTER DESIGN

A parallel coupled line filter is used at the output. In order to have a symmetrical filter the generator impedance is first changed to 50 ohms. The 20.6 ohm reactance is resonated with a 2 pF series capacitor. Then the 6.8 ohm generator is transformed to 50 ohms with a quarter wave line of 18.5 ohm characteristic impedance.

The number of filter elements is determined by the requirement that the filter attenuation be high at the input frequency. For n = 3 the isolation at 2 GHz is 37 dB. For n = 2 isolation is under 20 dB[7].

For n = 3 the prototype element values for a Chebyshev filter with 0.01 dB ripple are $g_1 = 0.629$, $g_2 = 0.970$, $g_3 = g_1$, $g_4 = 1 = g_0$[8]. For our normalized bandwidth of

$$\frac{4200\text{-}3800}{4000} = 0.1$$

these element values transform to the following impedance values[9] for a parallel coupled line filter operating between 50 ohm source and load.

$$(Z_{oe})_{01} = (Z_{oe})_{34} = 87.5 \text{ ohms}$$
$$(Z_{oo})_{01} = (Z_{oo})_{34} = 37.5 \text{ ohms}$$
$$(Z_{oe})_{12} = (Z_{oe})_{23} = 62 \text{ ohms}$$
$$(Z_{oo})_{12} = (Z_{oo})_{23} = 42 \text{ ohms}$$

From this data the width (W) and separation (S) of the coupled line filter can be computed[10].

$$W_{01} = W_{34} = 14 \text{ mils}$$
$$S_{01} = S_{24} = 4.8 \text{ mils}$$
$$W_{12} = W_{23} = 22.5 \text{ mils}$$
$$W_{12} = S_{23} = 16 \text{ mils}$$

When analyzed between 50 ohm generator and load, maximum SWR is 1.04. However, when the load is the resonated diode, the maximum SWR rises to 1.9. Optimizing the circuit elements reduces this maximum SWR to 1.6.

Since the load for the input and output filters is not simply the diode but includes the other filter behind the diode, the reflection coefficient doubles at some frequencies. Maximum input SWR over the 10% band is 1.17. Maximum output SWR is 2.92. Figure 4 shows the computer output for the complete multiplier.

Figure 5 is a sketch of the multiplier on 0.025 inch alumina microstrip.

CONCLUSION

Multiplier design techniques have been illustrated by a doubler to 4 GHz using Hewlett-Packard 5082-0805 step recovery diode. Using similar techniques a doubler with power output of 4 watts has been reported[11]. Bandwidth exceeded 10%. The procedure for higher order multipliers is similar, but the formula for equivalent diode resistance uses different constants[4].

```
COMPACT
COMMAND FILE ==> MULT
OST     AA    PA     20.00      -27.1          2000.
CAS     AA    AA
TRL     BB    SE     80.00      -15.10         2000.
OST     CC    PA     20.00      -58.1          2000.
CAS     CC    CC
TRL     DD    SE     80.00      - 4.6          2000.
OST     EE    PA     20.00      -30.           4000.
CAS     EE    EE
CAP     FF    PA      .2000
SRX     GG    PA     5.630       1.000          6.000
CAP     HH    SE     2.000
TRL     II    SE    -21.6       90.00          4000.
CPL     KK    MS    -10.5       - 2.9          289.0    9.600    25.00
CPL     LL    MS    -21.4       - 8.1          289.0    9.600    25.00
CON     KK    T4     1.000       2.000          3.000    4.000
CON     LL    T4     3.000       5.000          6.000    7.000
CON     LL    T4     6.000       8.000          9.000   10.000
CON     KK    T4     9.000      11.00          12.000   13.00
DEF     JJ    T2     1.000      12.00
CAX     AA    JJ
PRI     AA    S1    50.00
END
1800    2200   50
3600    4400   100
END
```

FREQUENCY	S_{11}	S_{21}	S_{12}	S_{22}	
1800.00	.23< 49	.00<- 94.5	.001<- 97.4	1.00<- 78	-63.54
1850.00	.14< 25	.00<-101.4	.001<- 84.1	1.00<- 81	-62.70
1900.00	.08<- 13	.00<-107.8	.001<-107.8	1.00<- 84	-61.83
1950.00	.07<- 63	.00<-113.8	.001<-107.1	1.00<- 87	-60.87
2000.00	.06<- 96	.00<-119.8	.001<-119.8	1.00<- 90	-59.78
2050.00	.04<-103	.00<-126.3	.001<-126.3	1.00<- 94	-58.51
2100.00	.04<- 28	.00<-134.0	.001<-137.5	1.00<- 97	-57.10
2150.00	.13<- 10	.00<-143.3	.002<-146.9	1.00<-100	-55.60
2200.00	.28<- 20	.00<-154.9	.002<-154.0	1.00<-104	-54.17
3600.00	1.00<-155	.02<- 9.0	.020<- 9.0	.91< 16	-33.94
3700.00	1.00<-157	.04<- 49.4	.036<- 49.4	.74<- 48	-28.87
3800.00	1.00<-158	.05<-101.0	.052<-101.0	.42<-140	-25.72
3900.00	1.00<-160	.06<-150.0	.058<-150.0	.23< 102	-24.74
4000.00	1.00<-161	.06< 166.5	.061< 166.5	.14<- 15	-24.35
4100.00	1.00<-162	.06< 122.5	.061< 122.5	.18<-179	-24.24
4200.00	1.00<-163	.06< 77.2	.055< 77.2	.49< 87	-25.18
4300.00	1.00<-164	.04< 37.3	.043< 37.3	.74< 24	-27.42
4400.00	1.00<-165	.03< 6.8	.031< 6.8	.87<- 23	-30.04

Figure 4. Computer Analysis of Multiplier

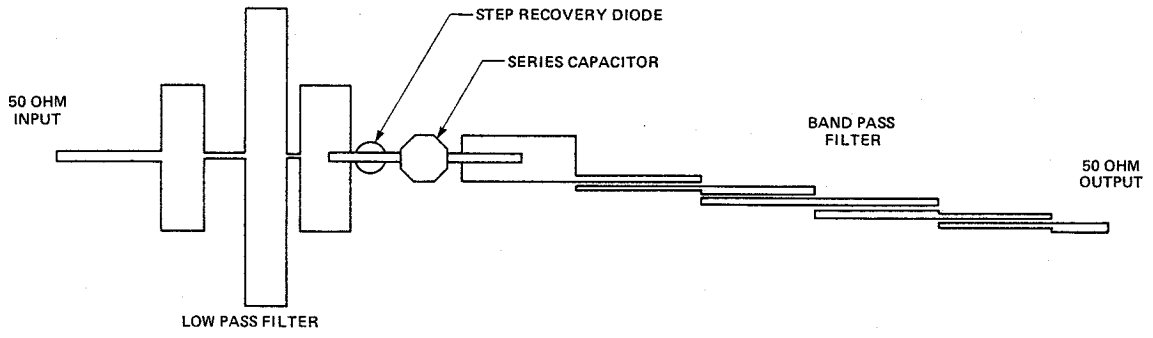

Figure 5. Microstrip Doubler

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