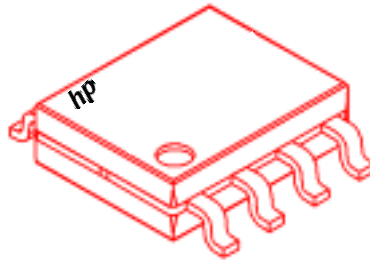


DC - 16 GHz Packaged Divide-by-2 Prescaler

Technical Data

HMMC-3102



Features

- **Wide Frequency Range:**
0.2–16 GHz
- **High Input Power Sensitivity:**
On-chip pre- and post-amps
-20 to +10 dBm (1–10 GHz)
-15 to +10 dBm (10–12 GHz)
-10 to +5 dBm (12–15 GHz)
- **P_{out} : +6 dBm (0.99 V_{p-p}) will drive ECL**
- **Low Phase Noise:**
-153 dBc/Hz @ 100 kHz Offset
- **(+) or (-) Single Supply Bias with wide range:**
4.5 to 6.5 V
- **Differential I/O with on-chip 50Ω matching**

Description

The HMMC-3102 is a packaged GaAs HBT MMIC prescaler which offers DC to 16 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Package Type: 8-lead SSOP Plastic
 Package Dimensions: 4.9 × 3.9 mm Typ.
 Package Thickness: 1.55 mm Typ.
 Lead Pitch: 1.25 mm Nom.
 Lead Width: 0.42 mm Nom.

Absolute Maximum Ratings[1]

(@ T_A=25°C, unless otherwise indicated)

Symbol	Parameters/Conditions	Min.	Max.	Units
V _{CC}	Bias Supply Voltage		+7	volts
V _{EE}	Bias Supply Voltage	-7		volts
V _{CC} - V _{EE}	Bias Supply Delta		+7	volts
V _{Logic}	Logic Threshold Voltage	V _{CC} -1.5	V _{CC} -1.2	volts
P _{in} (CW)	CW RF Input Power		+10	dBm
V _{RFIn}	DC Input Voltage (@ RF _{in} or RF _{in} Ports)		V _{CC} ± 0.5	volts
T _{BSS} [2]	Backside Operating Temp.	-40	+85	°C
T _{st}	Storage Temperature	-65	+165	°C
T _{max}	Maximum Assembly Temp. (60 seconds max.)		310	°C

[1] Operation in excess of any parameter limit (except T_{BSS}) may cause permanent damage to the device.

[2] MTTF > 5 × 10⁵ hours @ T_{BSS} < 85°C. Operation in excess of maximum operating temperature (T_{BSS}) will degrade MTTF.

DC Specifications/Physical Properties

($T_A = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 5.0$ volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	volts
$ I_{CC} $ or $ I_{EE} $	Bias supply current	68	80	92	mA
$V_{RFIn(q)}$ $V_{RFOut(q)}$	Quiescent DC voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	$V_{CC} - 1.45$	$V_{CC} - 1.35$	$V_{CC} - 1.25$	volts

[1] Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

($T_A = 25^\circ\text{C}$, $Z_0 = 50\Omega$, $V_{CC} - V_{EE} = 5.0$ volts)

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
$f_{in(max)}$	Maximum input frequency of operation	16	18		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] ($P_{in} = -10$ dBm)		0.2	0.5	GHz
$f_{Self-Osc.}$	Output Self-Oscillation Frequency[2]		3.4		GHz
P_{in}	@ DC, (Square-wave input)	-15	>-25	+10	dBm
	@ $f_{in} = 500$ MHz, (Sine-wave input)	-15	>-20	+10	dBm
	$f_{in} = 1$ to 10 GHz	-15	>-25	+10	dBm
	$f_{in} = 10$ to 12 GHz	-10	>-15	+10	dBm
	$f_{in} = 12$ to 15 GHz	-4	>-10	+4	dBm
RL	Small-Signal Input/Output Return Loss (@ $f_{in} < 12$ GHz)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ $f_{in} < 12$ GHz)		30		dB
ϕ_N	SSB Phase noise (@ $P_{in} = 0$ dBm, 100kHz offset from a $f_{out} = 1.2$ GHz Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing ($f_{in} = 10$ GHz, $P_{in} = -10$ dBm)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps
$P_{out[3]}$	@ $f_{out} < 1$ GHz	4	6		dBm
	@ $f_{out} = 2.5$ GHz	3.5	5.5		dBm
	@ $f_{out} = 3.5$ GHz	0	2.0		dBm
$ V_{out(p-p)} [4]$	@ $f_{out} < 1$ GHz		0.99		volts
	@ $f_{out} = 2.5$ GHz		0.94		volts
	@ $f_{out} = 3.5$ GHz		0.63		volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or RF_{in} (@ $f_{in} = 12$ GHz, Unused RF_{out} or RF_{out} unterminated)		-40		dBm
	f_{out} power level appearing at RF_{in} or RF_{in} (@ $f_{in} = 12$ GHz, Both RF_{out} & RF_{out} terminated)		-47		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or RF_{out} (@ $f_{in} = 12$ GHz, $P_{in} = 0$ dBm, Referred to $P_{in}(f_{in})$)		-23		dBc
H_2	Second harmonic distortion output level (@ $f_{out} = 3.0$ GHz, Referred to $P_{out}(f_{out})$)		-25		dBc

[1] For sine-wave input signal. Prescaler will operate down to D.C. for square-wave input signal. Minimum divide frequency limited by input slew-rate.

[2] Prescaler can exhibit this output signal under bias in the absence of an RF input signal. This condition can be eliminated by use of the Input DC offset technique described on page 3.

[3] Fundamental of output square wave's Fourier Series.

[4] Square wave amplitude calculated from P_{out}

Applications

The HMMC-3102 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 16 GHz bandwidth. Below 200 MHz

the prescaler input is "slew-rate" limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square-wave. AC coupling at P_{in} 5 (RF_{in}) is recommended for most applications.

The device can be operated from either a single positive or single negative supply. For positive supply operation V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with P_{in} 8 (V_{EE}) grounded. For negative

bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to P_{in} 8 (V_{EE}).

Input DC Offset

To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV DC offset voltage between the RF_{in} and \overline{RF}_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

GaAs MMICs are ESD sensitive. Proper precautions should be used when handling these devices.

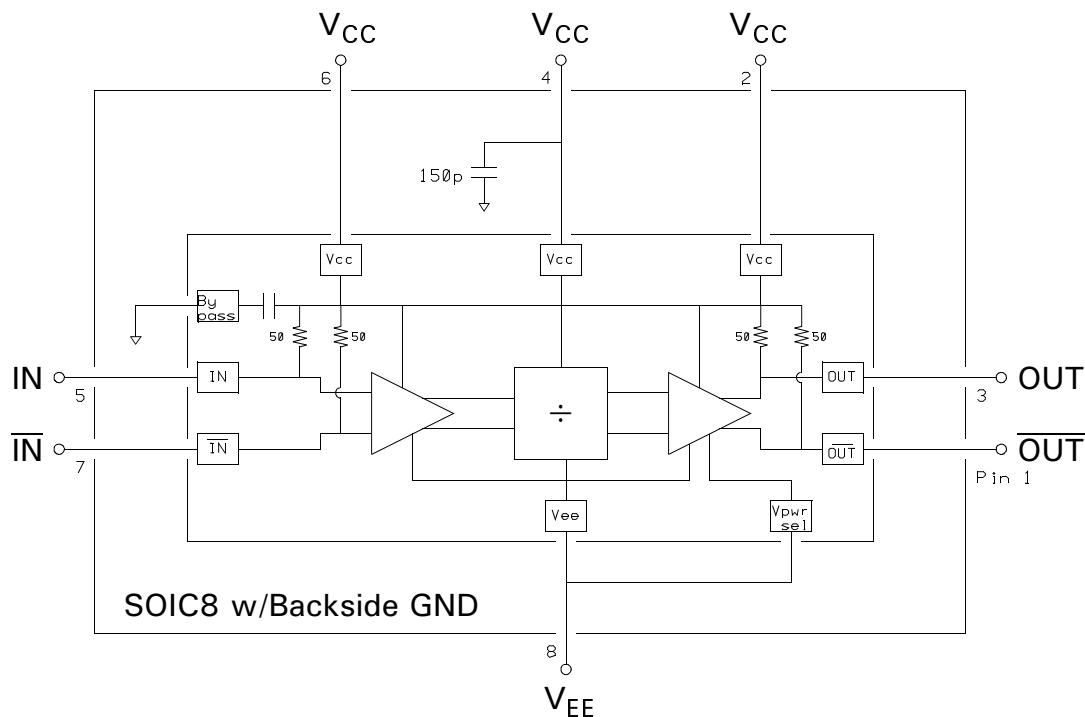
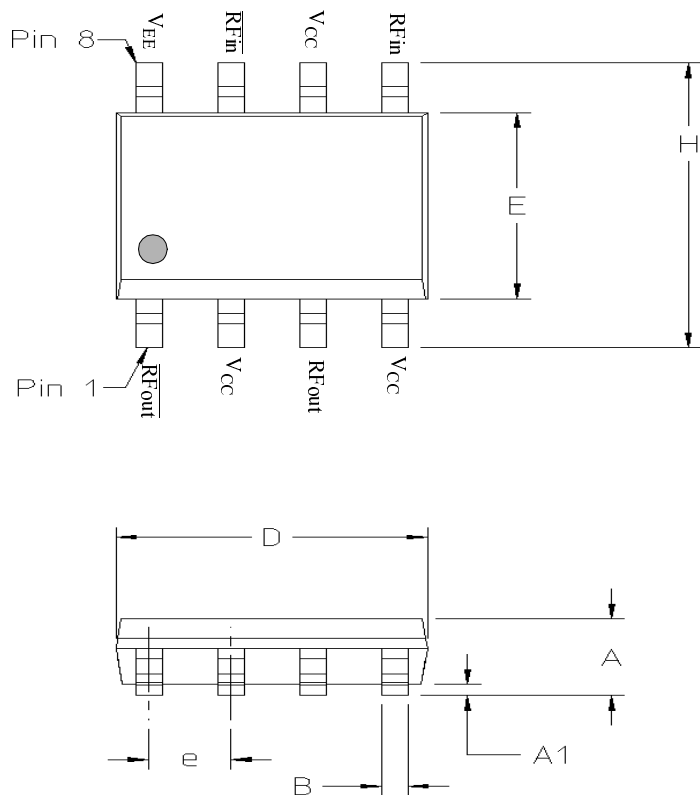


Figure 1.
Simplified Schematic



Notes:

- All dimensions in millimeters.
- Refer to JEDEC Outline MS-012 for additional tolerances

SYMBOL	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	.025
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.27
a	0°	8°

- Exposed heat slug area on pkg bottom = 2.67×1.65 .

Figure 2.
Package & Dimensions

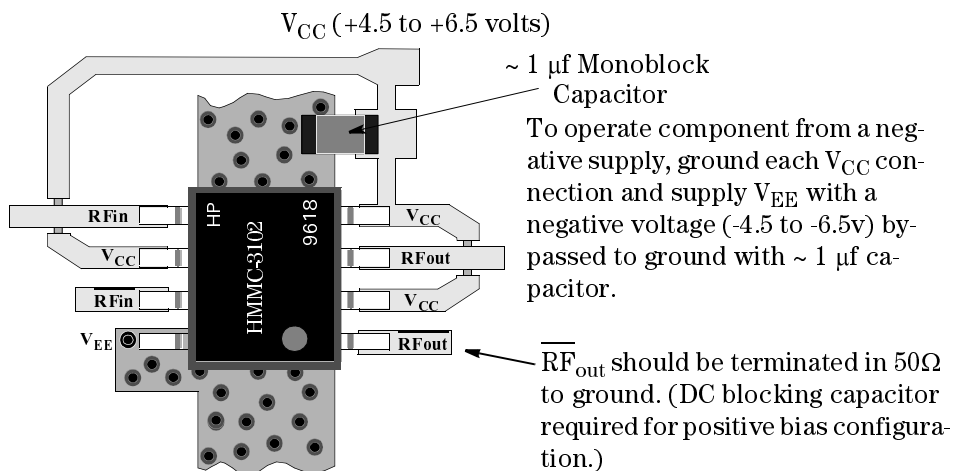


Figure 3.
Assembly Diagram
(Single-Supply, positive-bias configuration shown)

Supplemental Data:

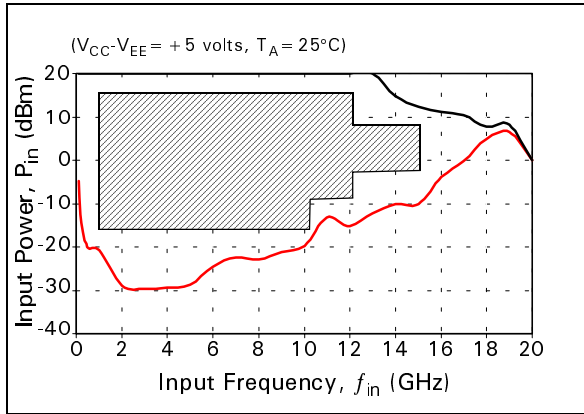


Figure 4.
Typical Input Sensitivity Window

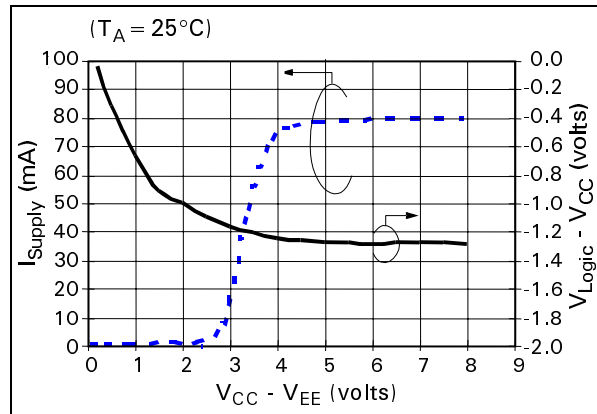


Figure 5.
Typical Supply Current & V_{Logic} vs. Supply Voltage

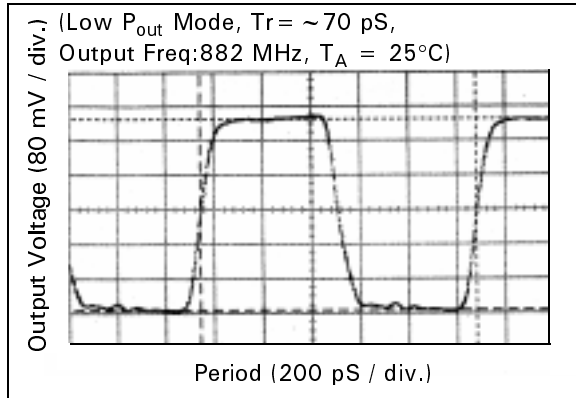


Figure 6.
Typical Output Voltage Waveform

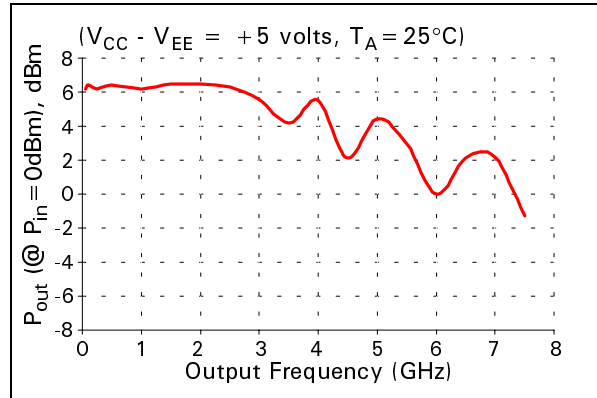


Figure 7.
Typical Output Power vs. Output Frequency, f_{out} (GHz)

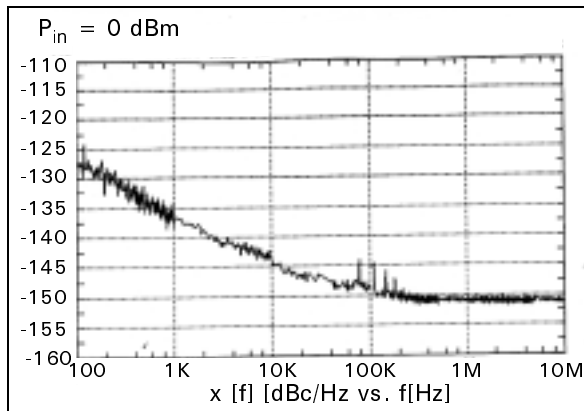


Figure 8.
Typical Phase Noise Performance

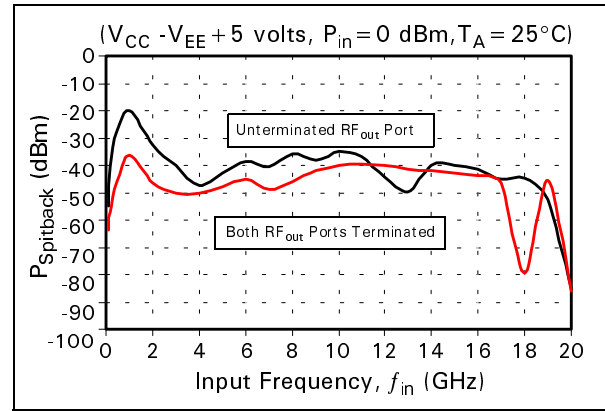


Figure 9.
Typical "Spitback" Power $P(f_{out})$ appearing at RF input port

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local HP sales representative.

Notes: